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(54) Device for implementation of DECT encryption algorithm with reduced current consumption

(57) The invention has application to the implementation of the DECT standard data ciphering algorithm which requires a lengthy procedure of key loading and logic operations during the stages of pre-ciphering and ciphering and requiring clocks operating at different frequencies.

This device performs parallel mode loading of the shift registers, with a ciphering keyword. It also calculates, in a first cycle, during the pre-ciphering, the values of the bits of each shift register that determine the value of the next shift in order to, in a second cycle, effect parallel mode shifting in these registers with a value equal to the sum of the two previous shift values.

During the ciphering process, the shifting is done in the registers, in parallel mode and in a single data clock cycle, with a value equivalent to the serial value obtained by the algorithm.

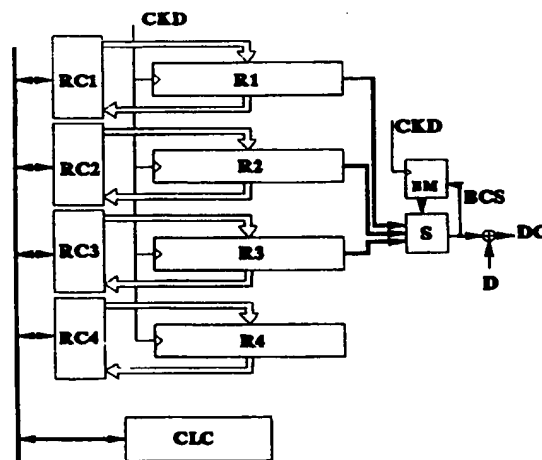


FIG. 5



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EUROPEAN SEARCH REPORT

Application Number
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			TECHNICAL FIELDS SEARCHED (Int.CI.6)
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 15 September 1999	Examiner HOLPER, G
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document</p> <p>T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons A: member of the same patent family, corresponding document</p>			

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ON EUROPEAN PATENT APPLICATION NO.**

EP 94 11 9371

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